13. The transistor device according to claim **1**, wherein the emitter comprises a metal material, the device further including an emitter transition layer configured to provide an insulating tunnel injection structure disposed at the emitter interface with the graphene material base layer (emitter/base interface).

14. The transistor device according to claim **1**, wherein the collector comprises an N-type semiconductor material.

15. The transistor device according to claim **1**, wherein the collector comprises one or more of ZnO, BN, InGaN, InAsP, InP, InGaAs, InAlAs, InGaSb, Diamond, GaN, GaAs, Silicon, 4H—SiC, GaSb, Germanium, Graphene, AlP, ZnS, GaP, AlSb, AlAs, InGaN, and MN material layers.

16. The transistor device according to claim **1**, wherein the collector is deposited on a substrate.

17. The transistor device according to claim **1**, wherein the graphene material base layer comprises N-type graphene.

18. The transistor device according to claim **1**, wherein the graphene material base layer comprises P-type graphene.

19. The transistor device according to claim **1**, wherein the graphene material base layer comprises a layered structure of a plurality of graphene sheets, a graphene sheet adjacent to the emitter being configured to facilitate the growth of emitter material on the graphene material base layer first side.

20. The transistor device according to claim **1**, wherein the graphene material base layer comprises a layered structure of a plurality of graphene sheets, a graphene sheet adjacent to the emitter being configured to improve interaction of the graphene material with a material forming the emitter.

21. The transistor device according to claim **1**, wherein the graphene material base layer comprises a layered structure of a plurality of graphene sheets, a graphene sheet adjacent to the emitter being configured to improve growth of emitter material on the graphene material base layer.

22. The transistor device according to claim **1**, wherein the graphene material base layer comprises a layered structure of a plurality of graphene sheets, a graphene sheet adjacent to the collector being configured to improve interaction of the graphene material with a material forming the collector.

23. The transistor device according to claim **1**, further comprising an emitter transition layer within the emitter disposed at the emitter interface with the graphene material base layer (emitter/base interface) and forming an interface with each of the emitter and the graphene material base layer;

wherein the emitter transition layer is configured to provide one of a thermionic emission injection structure, a planar doped barrier thermionic emission injection structure, a camel thermionic emission injection structure, a graded bandgap thermionic emission structure, a N-type/i-layer/P-type/i-layer (NIPI) doping superlattice injection structure, a superlattice injection structure, a tunneling injection structure, a metal-oxide tunnel injection structure, a Fowler Nordheim injection structure, a resonant tunneling injection structure, between the emitter and the graphene material base layer.

24. The transistor device according to claim **1**, further comprising a collector transition layer disposed at the collector interface with the graphene material base layer (collector/base interface) and forming an interface with each of the graphene material base layer and the collector;

wherein the collector transition layer is configured to smooth a conduction band potential barrier between the graphene material base layer and the collector and to facilitate the transport of electrons into the collector.

25. The transistor device according to claim **1** wherein the graphene material base forms a quantum well base having discrete allowed energy levels for the transit of electrons at the discrete allowed energy levels from the emitter to the collector.

26. The transistor according to claim **1** wherein current transits the graphene material base layer as ballistic electrons.

27. The transistor according to claim **1** where in the graphene material base layer has one of a graphene nanoribbon design having multiple graphene nanoribbons, an antidot design, a bi-layer material layer, and selected doping to introduce a bandgap into the graphene base material layer.

28. A transistor device comprising:

a graphene material base layer comprising at least one sheet of graphene;

a emitter adjacent to a first side of the graphene material base layer and forming an emitter/base interface therewith, the emitter having a conduction band minimum lower than a conduction band minimum of the graphene material base layer and being configured to inject electrons having an energy E less than a Fermi energy E_F of the graphene material base layer;

a collector adjacent to a second side of graphene material base layer opposite the first side and forming a collector/base interface therewith, the electron collector having a conduction band minimum lower than the conduction band minimum of the graphene material base layer and being configured to receive electrons from the graphene material base layer; and

a plurality of electrodes, each of the plurality of electrodes being connected to and forming a separate electrical connection with one of the emitter, collector, and base.

29. The transistor device according to claim **28**, wherein the emitter comprises an N-type semiconductor material.

30. The transistor device according to claim **28**, wherein the emitter comprises one of CdSe, InAs, SnO2:F, InSb, ZnO, BN, CdTe, CdS, In2O3:Sn, InGaN, InAsP, InP, InGaAs, InAlAs, InGaSb, and diamond emitter material layers.

31. The transistor device according to claim **28**, wherein the collector comprises an N-type semiconductor material.

32. The transistor device according to claim **28**, wherein the collector comprises one of CdSe, InAs, SnO2:F, InSb, ZnO, BN, CdTe, CdS, In2O3:Sn, InGaN, InAsP, InP, InGaAs, InAlAs, InGaSb, graphene, and diamond material layers.

33. The transistor device according to claim **28**, wherein the graphene material base layer comprises P-type graphene.

34. The transistor device according to claim **28**, wherein the graphene material base layer comprises a layered structure of a plurality of graphene sheets, a graphene sheet adjacent to the emitter being configured to facilitate the growth of emitter material on the graphene material base layer first side.

35. The transistor device according to claim **28**, wherein the graphene material base layer comprises a layered structure of a plurality of graphene sheets, a graphene sheet adjacent to the emitter being configured to improve the interaction of the graphene material with a material forming the emitter.

36. The transistor device according to claim **28**, wherein the graphene material base layer comprises a layered structure of a plurality of graphene sheets, a graphene sheet adjacent to the collector being configured to improve interaction of the graphene material with a material forming the collector.

37. The transistor according to claim **28** where in the graphene material base layer has one of a graphene nanoribbon design having multiple graphene nanoribbons, an antidot